CLAIMS

1. A cubic memory array, comprising:

a substrate having a planar surface;

a plurality of first select-lines organized in more than one plane parallel to the planar surface;

a plurality of second select-lines formed in pillars disposed orthogonal to the planer surface of the substrate; and

a plurality of memory cells respectively coupled to the plurality of first and plurality of second select-lines.

2. An integrated circuit embedding the cubic memory array of claim 1.

3. A memory carrier including the cubic memory array of claim 1.

4. An electronic device configured to receive the memory carrier of claim 3.

5. An electronic device including the cubic memory array of claim 1.

6. The cubic memory array of claim 1 wherein at least one of the memory cells includes a control element in series with a memory storage element.

7. The cubic memory array of claim 6 wherein the memory storage element is formed along the edge of one of the pillars.

8. The cubic memory array of claim 6 wherein the memory storage element is an antifuse device.

9. The cubic memory array of claim 6 wherein the memory storage element is a tunnel junction device.

10. The cubic memory array of claim 6 wherein the memory storage element is either a silicide switch or a LeCombre switch device.

11. The cubic memory array of claim 6 wherein the memory storage element comprises a write/erase/write or re-writeable phase-change material.

12. The cubic memory array of claim 6 wherein the control element is formed along the edge of one of the first select-lines.

13. The cubic memory array of claim 12 wherein the control element is formed along at least two edges of the first select line that form a point thereby enhancing the electrical field during programming.

14. The cubic memory array of claims 12 wherein the first select line is serpentine shaped.

15. The cubic memory array of claim 6 wherein the control element is a tunnel junction device.

16. The cubic memory array of claim 6 wherein the control element is a diode.

17. The cubic memory array of claim 6 wherein both the control element and the memory storage element are tunnel junction devices and wherein the control element is sized larger than the memory storage element to provide sufficient current to change the state of the memory storage element.

18. The cubic memory array of claim 6 wherein the control element is a diode comprised of material selected from the group of semiconductor materials consisting of polysilicon, amorphous silicon, and microcrystalline silicon.

19. The cubic memory array of claim 18 wherein the diode is selected from the group consisting of a pn junction, a pin junction, a Zener junction, an avalanche, a tunnel junction, and a Schottky junction diodes.

20. The cubic memory array of claim 6 wherein the control element is selected from the group consisting of a recrystallized semiconductor, an amorphous semiconductor, a polycrystalline semiconductor, a junction field effect transistor, a junction field effect transistor with its gate connected to its source or drain, an insulated gate field effect transistor with its gate connected to its source or drain, a four-layer diode, an NPN transistor, and a PNP transistor.

21. The cubic memory array of claim 6 wherein the memory storage element is selected from the group consisting of an antifuse, a fuse, a charge storage device, a resistive material, a trap-induced hysterisis material, a ferroelectric capacitor material, a Hall effect material, and a tunneling magneto-resistive material.

22. The cubic memory array of claim 6 wherein the memory storage element is an antifuse including material from the group consisting of an oxidized metal tunnel junction, a silicon dioxide tunnel junction, a dielectric-rupture, a polysilicon semiconductor, a polycrystalline semiconductor, an amorphous semiconductor, a microcrystalline semiconductor, a metal filament electro-migration semiconductor, and a polysilicon resistor semiconductor.

23. The cubic memory array of claim 1, further comprising a switching element in the substrate electrically connected to at least one pillar and disposed substantially beneath the respective pillar.

24. A 3D-memory array on a substrate defining a plane, comprising:

a plurality of memory cells stacked vertically, comprising,

a dielectric layer forming an insulating surface

a first select-line disposed parallel to the plane of the substrate on the dielectric layer,

a control element surrounding the first select-line, and

a memory storage element at least partially surrounding the control element; and

a vertical pillar connected to a second select-line, substantially orthogonal to the plane of the substrate and contacting the memory storage element.

25. The 3D-memory array of claim 24 wherein the control element is a tunnel junction.

26. The 3D-memory array of claim 24 wherein the control element is a diode.

27. The 3D-memory array of claim 24 wherein the memory storage element is a tunnel junction.

28. The 3D-memory array of claim 24 wherein the memory storage element is a dielectric-rupture device.

29. The 3D-memory array of claim 24 wherein the vertical pillar has a first side contacting the memory storage element, further comprising:

an interlayer dielectric contacting a second side of the vertical pillar and extending a predefined distance; and

another plurality of memory cells stacked vertically disposed next to the interlayer dielectric at the predefined distance.

30. The 3D-memory array of claim 24 wherein the vertical pillar has a first side contacting the memory storage element, further comprising:

another plurality of memory cells stacked vertically and contacting a second side of the vertical pillar.

31. The 3D-memory array of claim 24 wherein the first select-line is layout in a serpentine fashion.

32. The 3D-memory array of claim 24 wherein the vertical pillar contacts the memory storage device over at least two surfaces.

33. The 3D-memory array of claim 24 further comprising a transistor formed in the substrate electrically connected to the vertical pillar and disposed substantially beneath the respective vertical pillar.

34. A method of creating a memory circuit, comprising the steps of:

forming an array of first select-lines in a plane substantially parallel to a substrate;

forming an array of second select-lines normal to plane of the first select-lines; and

forming an array of memory cells, each respectively coupled to a respective first and second select-line.

35. The method of claim 34 wherein the step of forming an array of memory cells further includes the step of contacting a memory storage device to one of the second select-lines.

36. The method of claim 34 where in the step of forming an array of memory cells further comprises the step of forming tunnel junction devices.

37. The method of claim 34 wherein the step of forming an array of memory cells further comprises creating a control element of doped semiconductor material.

38. The method of claim 34 wherein the step of forming an array of first select-lines further includes the step of forming a portion of the array of first select-lines in stacked vertical columns.

39. The method of claim 34 wherein the step of forming second select-lines normal to the plane of the first select-lines further includes contacting the memory cells in at least two edges that intersect.

40. The method of claim 34 further comprising the step of creating a transistor in the substrate disposed substantially adjacent to and that is coupled to at least one of the formed array of second select-lines.

41. A method of fabricating a memory circuit, comprising the steps of:

applying an insulator on a substrate;

applying a set of first conductors in one or more planes parallel to the substrate;

creating a set of control elements on respective first conductors;

applying a second conductor orthogonal to the planes of the first conductors; and

creating a set of memory storage elements between the second conductor and the respective control elements.

42 A method of fabricating a memory circuit of N-levels comprising repeating the steps of claim 41 N-times.

43. The method of claim 41 further comprising the step of planarizing the insulator after it is applied.

44. The method of claim 41 wherein the step of creating a set of control elements further includes the steps of:

oxidizing the set of first conductors; and

applying a set of patterned third conductors over the oxidized set of first conductors.

45. The method of claim 44 wherein the step of creating a set of memory storage elements further includes the step of oxidizing the sets of patterned third conductors.

46. The method of claim 45 wherein the step of oxidizing the set of patterned third conductor includes the step of creating a tunnel junction.

47. The method of claim 45 wherein the step of oxidizing the set of patterned third conductors includes the step of creating a dielectric-rupture device.

48. The method of claim 41 wherein the step of creating a set of control elements further includes the step of applying a dielectric layer on the set of first conductors.

49. The method of claim 41 wherein the step of creating a set of control elements further comprises the step of applying a variable doped semiconductor to form a set of diodes.

50. The method of claim 41 wherein the step of applying a set of second conductors further includes the step of applying a layer of tungsten.

51. The method of claim 41 wherein the step of applying a set of second conductors further includes the step of creating a set of vias defining the location of the set of second conductors in the insulator.

52. A memory circuit, comprising:

means for selecting a first select-line within an array of memory cells, said means disposed in a plane; and

means for selecting a second select-line within the selected array of memory cells, said means disposed in a direction normal to the plane of said means for selecting a first select-line.

53. The memory circuit of claim 52, further comprising:

means for controlling the path of current from the selected first select-line to the selected second select-line; and

means for storing a memory state disposed between said means for controlling and said selected second select-line.

54. The memory circuit of claim 53 wherein said means for controlling the path of current comprises a tunnel junction device.

55. The memory circuit of claim 53 wherein said means for storing a memory state is a tunnel junction device.

56. An integrated circuit embedding the memory circuit of claim 52.

57. A memory carrier including the memory circuit of claim 52.

58. An electronic device capable of accepting the memory carrier of claim 57.

59. An electronic device including the memory circuit of claim 52.

60. A computer comprising at least one memory circuit of claim 52.

61. A memory cell, comprising:

a vertical pillar extending from the bottom of the cell to the top of the cell;

a control element having a first cross sectional area;

a storage element having a second cross sectional area less than the first cross section area, the storage element in contact with the vertical pillar; and

a middle electrode coupling the control element to the storage element.

62. The memory cell of claim 61 wherein the storage element is angled to enhance an electrical field generated between the vertical pillar and the middle electrode.

63. The memory cell of claim 61 wherein the control element and the storage element are of the same type of device.

64. The memory cell of claim 63 wherein the type of device is a tunnel junction device.

65. The memory cell of claim 61 wherein the storage element is a write/erase/write storage element.

66. The memory cell of claim 61, further comprising:

a second vertical pillar extending from the bottom of the cell to the top of the cell;

a second control element having a third cross sectional area;

a second storage element having a fourth cross sectional area less than the third cross section area, the second storage element in contact with the second vertical pillar; and

a second middle electrode coupling the second control element to the second storage element.

67. A cubic memory array on a horizontal substrate surface, comprising:

a first set of horizontal select lines;

a second set of horizontal select lines;

a plurality of memory cells of claim 61 arranged in a stack of layers and interfacing to the first set of horizontal select lines and the plurality of memory cells forming extended vertical pillars coupled to the second set of horizontal select lines.

68. The cubic memory array of claim 67 further comprising a set of selection circuitry connected to the extended vertical pillars.

69. The cubic memory array of claim 68 wherein the set of selection circuitry is comprised of at least one diode or field effect transistor.

70. The cubic memory array of claim 69 wherein the each of the members of the set of selection circuitry is coupled to one or more extended vertical pillars.

71. A cubic memory array on a horizontal substrate surface, comprising:

a first set of horizontal select lines;

a second set of horizontal select lines;

a plurality of memory cells of claim 66 arranged in a stack of layers and interfacing to the first set of horizontal select lines and the plurality of memory cells forming extended vertical pillars coupled to the second set of horizontal select lines.